IN THE CLAIMS

Please amend the claims as follows:

1. (Canceled)

2. (Currently amended) A semiconductor device comprising: ~~according to claim 1,~~

an uppermost layer wiring formed on a semiconductor substrate;

a rewiring layer formed on said uppermost layer wiring through a protection film; and

a bump electrically connected to said rewiring layer, and formed within a region of said uppermost layer wiring,

wherein said bump is formed within a region of a wiring width of said uppermost layer wiring.

3-4. (Canceled)

5. (Currently amended) A semiconductor device comprising: ~~according to claim 3,~~

an uppermost layer wiring formed on a semiconductor substrate;

a rewiring layer formed on said uppermost layer wiring through a protection film; and

a bump electrically connected to said rewiring layer, and formed within a region of said uppermost layer wiring,

wherein said bump is formed inside of the sides of the uppermost layer wiring and ~~wherein said bump is~~ formed within a region of a wiring width of said uppermost layer wiring.

6-10. (Canceled)

11. (Currently amended) A method of designing a semiconductor device comprising: ~~according to claim 9~~,

an uppermost layer wiring formed on a semiconductor substrate,

a rewiring layer formed through a protection film and a bump connected to said rewiring layer,

wherein a process of arranging said bump comprises a step of:

arranging said bump so that it is located inside of the sides of said uppermost layer wiring, and

~~wherein the process of arranging said bump comprises a step of:~~

arranging said bump so that it is located within a region of a wiring width of said uppermost layer wiring.

12-13. (Canceled)

14. (Currently amended) A method of designing a semiconductor device comprising a step of arranging the uppermost layer element wiring structure described in claim 2 such that the uppermost layer element wiring structure is located beneath each of all bumps.

15-16. (Canceled)

17. (Currently amended) A method of designing a semiconductor device comprising a step of arranging the uppermost layer element wiring structure described in claim 5 such that the uppermost layer element wiring structure is located beneath each of all bumps.

18. (New) The semiconductor device according to claim 2, wherein all of the bumps in the semiconductor device are formed within a region of said uppermost layer wiring.